Calibrating Volatile Threshold Switching Memristor P-bits for Aligned Stochastic Outputs in Probabilistic Computing

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EMDS Emerging Materials, Device & System

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INTRODUCTION

❖ Combinatorial Optimization Problems (COPs)

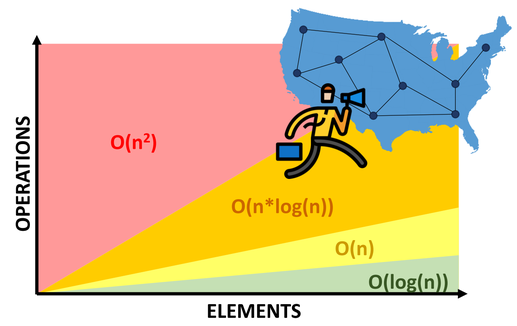
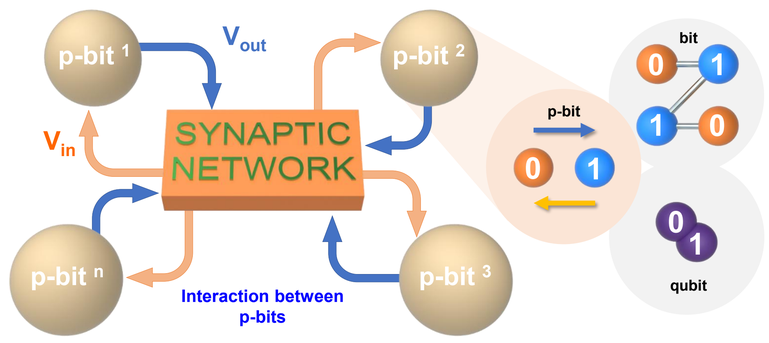
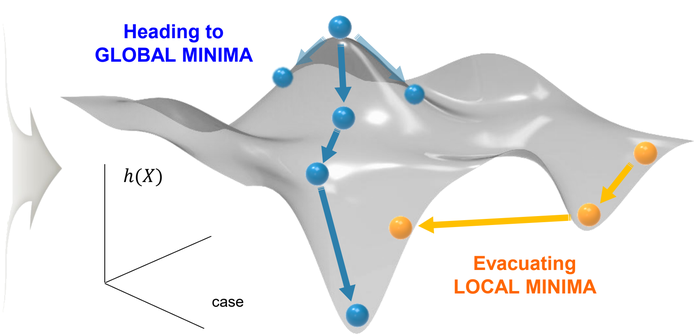


Image source : IBM

- ✓ **Combinatorial optimization problems (COPs)** typically exhibits exponential time complexity
- ✓ **Quantum annealing (QA)** have been proposed to solve COPs at high speed, **but requiring cryogenic environment**

❖ Probabilistic Computing: Energy Network-based Problem Solving

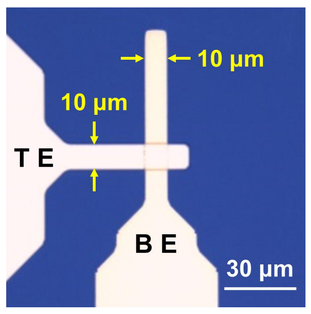


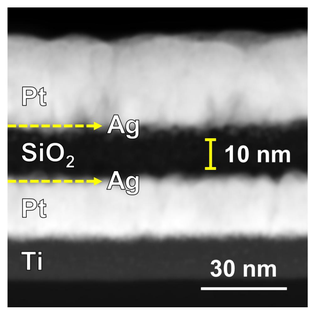


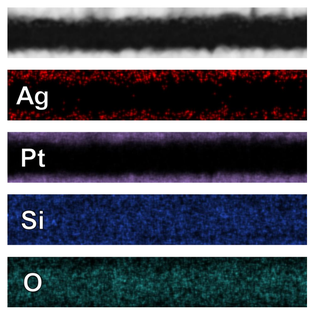
- ✓ **Probabilistic computing** has been proposed as an attractive approach for **solving COPs by mimicking QA at room temperature** using the stochastic output (0 or 1) of **probabilistic bit (p-bit)**
- ✓ However, achieving consistent output trends by altering the material system of the devices is not feasible
- ✓ An appropriate strategy is to **adjust the output probabilities by varying the signals applied to each p-bit**

DEVICE FABRICATION

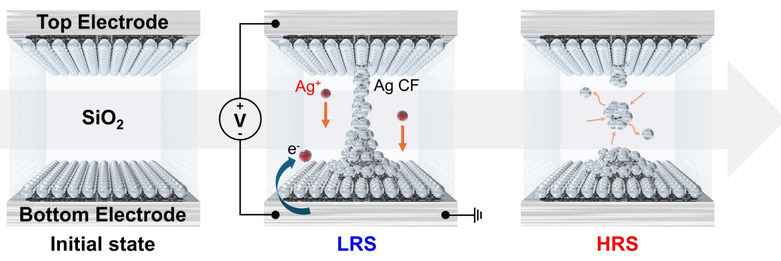
❖ Electro-Chemical Metallization based Volatile Memristor

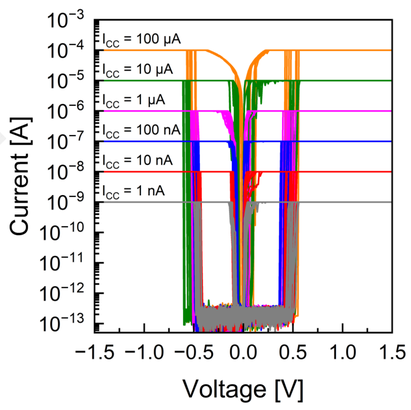






- ✓ Top/Bottom electrode (Ag/Pt) : E-beam evaporation
- ✓ Oxide layer (SiO_2) : RF magnetron sputtering



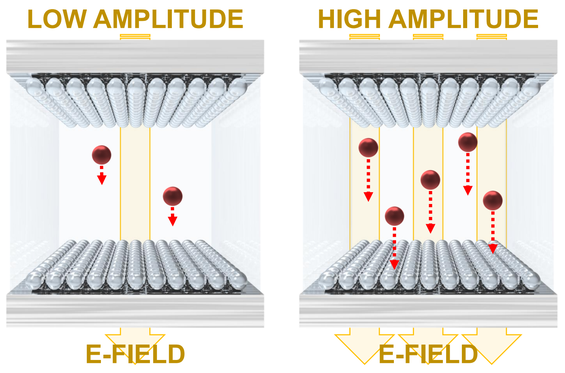


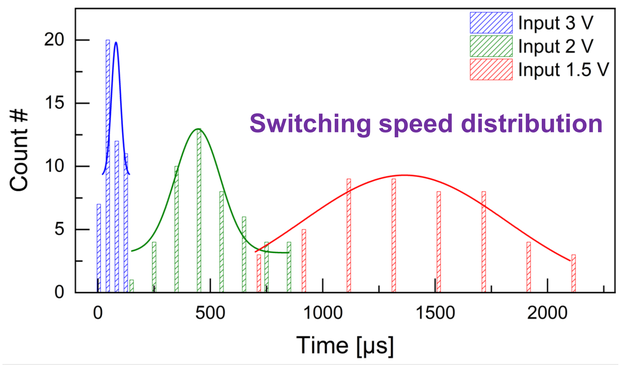
- ✓ Voltage bias applied (Low resistance state, **LRS**)
  → oxidized Ag^+ percolate through oxide layer
  → Ag^+ is reduced to Ag atoms at the opposite electrode
  → Accumulated Ag forms **conductive filament (CF)**
- ✓ Zero biased (High resistance state, **HRS**)
  → CF **voluntarily ruptures** due to the surface energy minimization

$V_{th} \approx \pm 0.5$ [V]
OFF current < 1 [pA]
ON / OFF ratio > 10^8

P-BIT IMPLEMENTATION

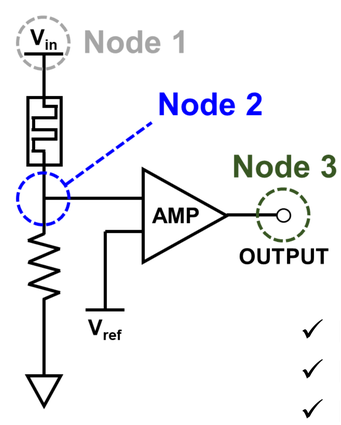
❖ Amplitude-dependent Switching Speed Variation

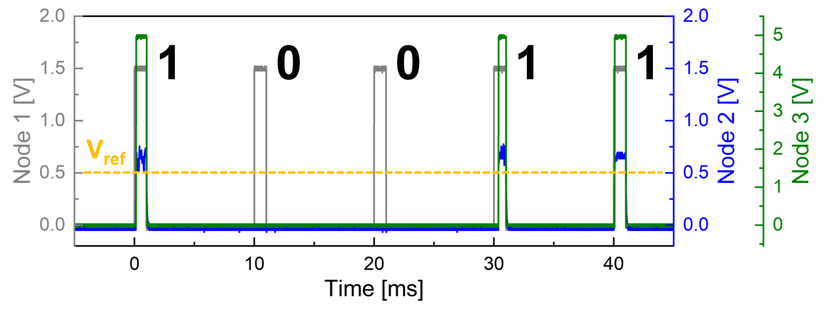




- ✓ Stronger the electric field (higher the input pulse amplitude), faster the switching speed
- ✓ Wider the input pulse width, higher the switching probability

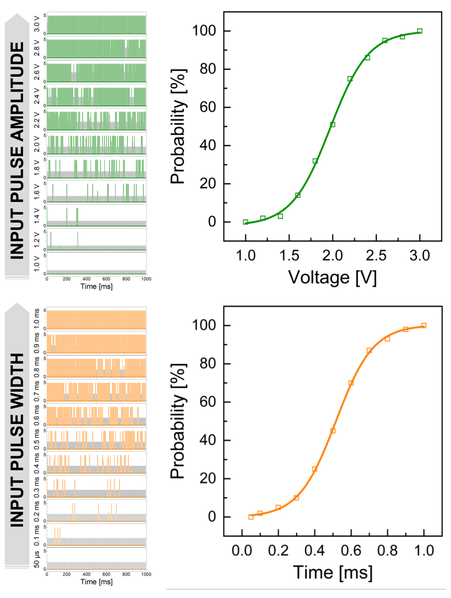
❖ Circuit Construction for p-bit

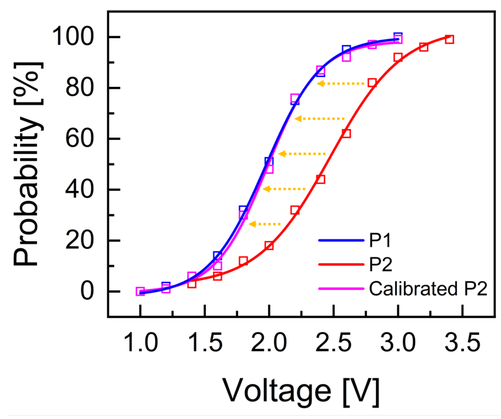




- ✓ Node 1: Input pulse applied to volatile memristor
- ✓ Node 2: Probabilistic signal generation by stochastic switching
- ✓ Node 3: Refined output signal generation through OP-AMP

CALIBRATION STRATEGY

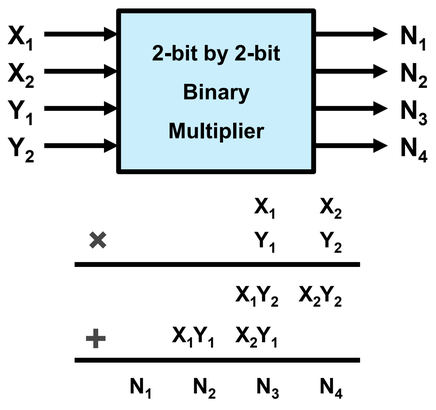




- ✓ By either fixing the pulse width and increasing the pulse amplitude, or fixing the amplitude and increasing the pulse width, stochastic output with tunable probability (sigmoid fitted curve) is achieved
- ✓ For two p-bits (P1 and P2) with large device-to-device variation, P2 was calibrated by increasing the input pulse width
- ✓ After calibration, **the sigmoid curves of P1 and P2 exhibited aligned stochastic output characteristics (less than 5 percentage points over all step amplitudes)**

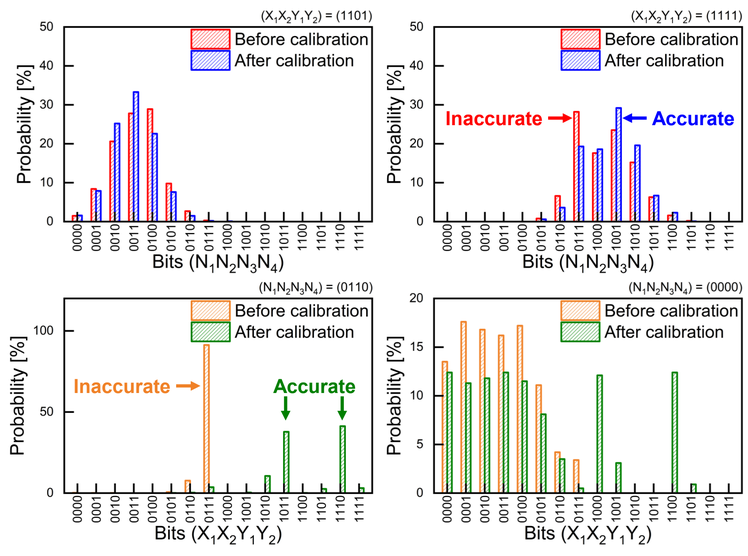
PROBLEM SOLVING DEMO

❖ Forward & Inverse Operation of Binary Multiplier



$$\begin{array}{cccc} & & X_1 & X_2 \\ \times & & Y_1 & Y_2 \\ \hline & & X_1Y_2 & X_2Y_2 \\ + & X_1Y_1 & X_2Y_1 & \\ \hline N_1 & N_2 & N_3 & N_4 \end{array}$$

Sequential logic can be reconfigured as COP based on its truth table



- ✓ Prior to calibration (employing P1 + P2): **Fails to perform accurate computation**
- ✓ After the calibration (employing P1 + Calibrated P2): **Successfully rendering output probabilities for both forward & inverse operations**

CONCLUSION

- ✓ This study demonstrated the feasibility of implementing calibrated p-bits using volatile memristors for probabilistic computing
- ✓ The probability of p-bit outputs depends on pulse amplitude and pulse width was verified through sigmoid curve fitting, demonstrating the capability of a p-bit with a simple structure.
- ✓ A calibration strategy was applied to address output inconsistencies caused by device-to-device variations in the volatile memristors
- ✓ This strategy involved adjusting input signal parameters, such as amplitude and pulse width, ensuring consistent output probabilities and reliable functionality across multiple p-bits
- ✓ The transition from an uncalibrated to a calibrated p-bit allowed for consistent performance in both the forward and inverse operations of the binary multiplier reconfigured as COP

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